EXHIBIT A

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BY FEDEX

Babak Sani, Esq.
Townsend, Townsend & Crew
Two Embarcadero Center, 8th Floor
San Francisco, CA 94111

Re: Invention Disclosure entitled:
Flip Chip Attach and Copper Clip Attach on MOSFET Devices
Inventors: Maria Cristine B. Estacio, Maria Clemens Y. Quinones
Our Reference No.: 17732-1394

Dear Babak:

Enclosed is the above entitled invention disclosure for drafting into a patent application. Feel free to contact the inventors directly, but make sure that you copy me on any e-mails or written correspondence with a copy also to Chris Caseiro at Pierce Atwood.

I have committed to our management and patent committee that all patent applications will be promptly prosecuted. To this end, if you can't make contact in two weeks and expeditiously pursue the application, please let me know as soon as possible.

Thanks for your assistance.

Best regards,

Daniel E. Boxer

cc: Maria Cristine B. Estacio
Maria Clemens Y. Quinones
Consuelo Tangpuz
Steve Sapp
Chris Caseiro, Esq.

RECEIVED

[redacted]

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Invention Disclosure

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Please complete each item of this form. If an item is not applicable, enter "N/A"

General Information Concerning the Invention

Title of invention: *Flip Chip Attach and Copper Clip attach on MOSFET devices*

Brief description of the invention: *The objective of the invention is to define an assembly process that will meet very low package resistance (RDSon) for MOSFET devices on any given surface-mount discrete package with superior thermal performance and which can be manufactured on a high-volume environment. The invention combines the flip chip attach and copper clip attach approach in one. The bumped die is flipchip attached on the leadframe for source and gate connection while the drain connection is taken cared by the clip soldered on the die backside. This new packaging concept can lower the overall package resistance significantly as the design can now cater to bigger die sizes and thinner dice up to 4 mils with more reliable connections. The final part will still have the same size and footprint as the standard package.*

Below details the assembly process flow:

Wafer Saw
|
Flipchip attach (See Figure 1, steps 1 & 2)
|
Clipbonding (See Figure 1, steps 3 & 4)
|
Encapsulation
|
Degate / Debar / Deflash
|
Marking
|
Solder Plating
|

Trim & Form

Test/ Pack

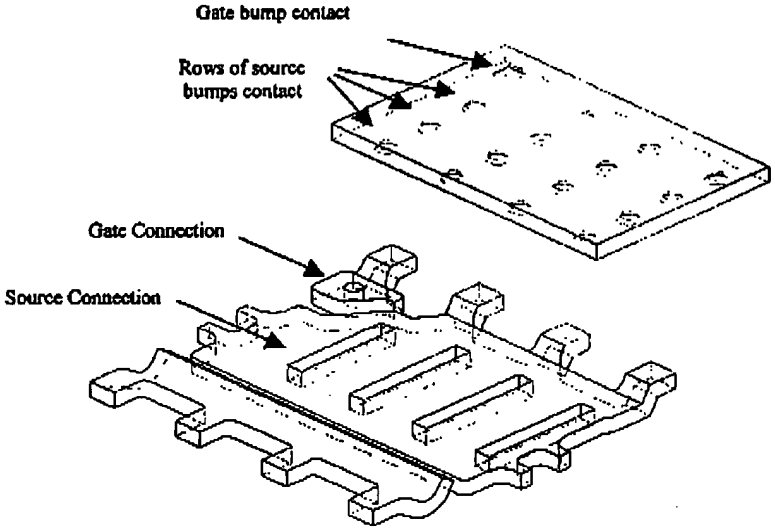
Construction Details: (Refer to Figure 1)

Attach photocopies of all pertinent documentation. Each page must be signed, dated, and witnessed by two other persons who have read and understood the description of the invention.

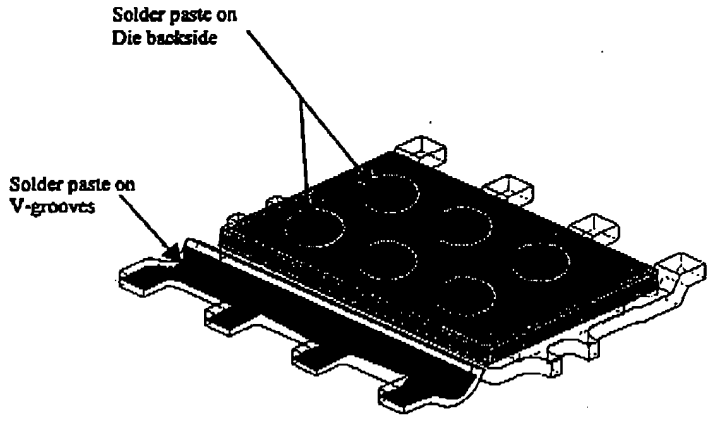
FIGURE 1 . Process Flow

Option 1. One time reflow of the bumps and copper clip
Option 2. Reflow after flipchip attach, then another reflow after clip attach

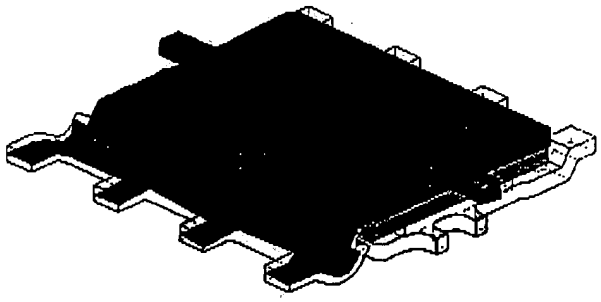
Step 1. Bumped die from the wafer on a sawn tape is flipchip attached on the gate and source frame (flux application could either be through bump dipping or flux dispensing on the gate/source frame):



Step 2: Dispensing of the solder paste on the die backside and the V-grooves:



Step 3. Pick-and-place of the copper clip (supplied in reel form) unto the die backside and v-grooves



Step 4. Reflow to solder the bumps on the gate/source frame and at the same time, solder Copper clip to the die backside and the v-groove for the drain connection.